REMARKS

Claims 67-116 are pending in the present application.

In the office action mailed December 16, 2005 (the "Office Action"), the Examiner rejected claims 67-80 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,950,956 to Zerbe *et al.* (the "Zerbe patent") and further rejected claims 67-80 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,910,146 to Dow (the "Dow patent"). Claims 67-116 were also rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-66 of U.S. Patent No. 6,801,989 to Johnson *et al.* (the "Johnson patent").

An information disclosure statement was submitted on October 14, 2003 (the "IDS"). Applicants request the Examiner consider the references cited in the Form PTO-1449 of the IDS and provide the attorney of record with a signed and initialed copy of the Form PTO-1449.

Claim 74 has been amended to more clearly recite the subject matter of the claimed invention. It will be apparent from the amendment, and the comments below, that the amendment to claim 74 was made independent of the cited references. The previously mentioned amendment does not narrow or further limit the scope of the invention as recited by unamended claim 47. Generally, the amendment makes explicit what is implicit in the claim and adds language that is inherent in the unamended claim. Consequently, the amendment to claim 74 should not be construed as being "narrowing amendment," because it was not made for a substantial reason related to patentability.

With respect to the rejection of claims 67-116 under the judicially created doctrine of obviousness-type double patenting over claims 1-66 of the Johnson patent, a timely filed terminal disclaimer in compliance with 37 C.F.R. 1.321(c) has been provided with this amendment. Consequently, the rejection of claims 67-116 for obviousness-type double patenting should be withdrawn.

Claims 67-80 are patentably distinct from the Zerbe patent and also patentably distinct from the Dow patent because neither patent discloses the combination of limitations recited by the respective claim.

The Zerbe patent discloses circuits and methods for adjusting the timing of data signals between a master device and slave devices. As pointed out by the Zerbe patent, various factors can affect the timing of the data signals. These factors, however, can be adjusted using the various embodiments described in the Zerbe patent. Namely, the Zerbe patent describes embodiments for signal timing adjustment, duty cycle adjustment, adjustment to correct voltage errors, and signal equalization. The material cited by the Examiner as the basis for anticipating claims 67-80 is related to signal timing adjustment described by the Zerbe patent, which will now be discussed in greater detail.

Several examples of signal timing adjustment are described in the Zerbe patent for providing timing error compensation, both for read and write operations between a master device and individual slave devices. Compensation is provided by adjusting phase relationships of internal transmit and receive clock signals (TCLK and RCLK) relative to clock-to-master (CTM) and clock-from-master (CFM) clock signals, respectively, of a folded clock signal. Figures 7-11 illustrate various embodiments of circuits that are used to alter the timing of the TCLK and RCLK signals relative to the CTM and CFM clock signals. These embodiments utilize various techniques to change the timing relationship, for example, a phase mixer combining three-clock signals to provide adjustment over a range of –45 degrees to +45 degrees. Other embodiments alter the TCLK and RCLK relative timing by adding or subtracting capacitive loads to a series of inverters, utilizing binary-weighted current sources to provide an offset current to the differential input of PLL/DLL phase detector, using a DLL having delay elements that can be adjusted based on supply voltage and adjusting the supply voltage to provide a desired delay, and using a pair of interpolator circuits (a primary interpolator and an offset interpolator) to generate an output clock signal that is adjusted according to an offset value. Whatever technique is used, the resulting TCLK and RCLK signals are then applied to the transmitters 70 and the receivers 60, respectively, so that data is transmitted and latched by the slave device 12 at the proper times relative to the CTM and CFM signals.

The Dow patent describes a technique for determining the amount of signal timing adjustment to set for the TCLK and RCLK signals relative to a master clock signal. The TCLK and RCLK signals are internal clock signals for timing the transmission and reception of data by the IC dies 110. The TCLK and RCLK signals are generated in response to a differential

outbound clock signal OUTCLK/OUTCLKN and a differential inbound clock signal INCLK/INCLKN, respectively, of the master clock signal. Figure 4 illustrates a flow diagram for testing a range of different TCLK times relative to the OUTCLK/OUTCLKN signals and Figure 5 illustrates a flow diagram for testing a range of different RCLK times relative to the INCLK/INCLKN signals. A table of pass/fail results for various combinations of different TCLK and RCLK times can be generated using the processes described with reference to Figures 4 and 5. Examples of pass/fail tables are shown in Figures 6 and 7. Based on the table of results, optimum TCLK/RCLK timing conditions can be set for a IC die. Registers 137 and 139 store the delay values representing the optimum TCLK and RCLK timing conditions. The Dow patent further describes a process for improving timing margin between IC dies by adjusting the strength of a pull down or pull up transistor on the data and clock lines, adjusting the clock to data skew, and adjusting a reference voltage that is used to determine the logic value of an input signal.

The Zerbe and Dow patents fail to disclose the combination of limitations recited by claims 67-80 because neither patent describes individually adjusting the timing of data signals relative to a reference clock. As described in the present application, the time at which each data signal is valid (i.e., the data eye) should overlap enough so that, in the case of reading data from a memory device, the memory controller can latch all of the data at one instance. In an extreme case, the data eye of at least one of the data signals does not overlap with the data eye of any other signal, resulting in a situation where it is impossible to latch all bits of data at one instance. This situation is illustrated in Figure 4 and described at page 11, line 14-page 12, line 11 of the present application. In order to avoid non-overlapping data eyes, embodiments of the invention provide *individual* timing adjustment for a plurality of the data signals relative to a reference clock. As a result, the timing of the data eyes for different data signals are adjusted relative to one another to provide sufficient overlap for all bits of the data to be valid at one instance. In one embodiment described in the present application, each of the output data latches is clocked by a respective clock signal that is tailored to the timing skew for that particular data signal. A clock generator generates a plurality of clock signals having different phases relative to a reference clock signal. For each of the output data latches, one of the plurality of clock signals is selected through a testing process to clock the respective latch and a value that is indicative of

the respective selection is stored. The selected signal is then used to clock the output data latch for that data signal.

Claims 67 and 74 recite limitations that highlight the individual adjustability of at least two data signals of a plurality of data signals. For example, claim 67 recites a method including, among other things, determining a level of timing compensation for *each* of the respective internal clock signals to compensate for the *respective* signal skew determined for *each* of the two digital signals for at least two of the plurality of digital signals. Additionally, the method of claim 67 further includes storing for *each of the two digital signals* a respective value indicative of the level of compensation for *each of the respective internal clock signals*, and adjusting the timing of *each of the respective internal clock signals* relative to the common clock signal according to *the respective value stored for each of the two digital signals*.

As previously discussed, neither the Zerbe or Dow patents disclose adjusting the timing of at least two of the data signals of a plurality of data signals relative to a common clock signal. Both the Zerbe and Dow patents disclose and contemplate adjusting the TCLK signal and using the adjusted TCLK signal for adjusting the timing of all of the transmitted data signals and further adjusting the RCLK signal and using the adjusted RCLK signal for adjusting the timing of all of the received data signals. The Zerbe and Dow patents address the problem of timing skew between the TCLK and the CTM clock and timing skew between the RCLK and the CFM clock. However, the inventions described in the Zerbe and Dow patents do not address the problem of timing skew between the data signals themselves. This can be illustrated by the fact that adjusting either the TCLK and/or RCLK according the Zerbe or Dow patent cannot change the timing of the data eyes of the separate data signals relative to one another. In contrast, *individual* timing adjustment of at least two data signals is recited in the method of claim 67 can be used to address this problem.

Similarly, claim 74 recites limitations that are directed to providing separate timing adjustments to at least two data signals of a plurality of data signals. Claim 74 recites a method that includes selecting one of the plurality of phase adjusted clock signals to act as the respective timing clock signal in order to compensate for the respective timing skew of the digital signal for *each of at least two* of the plurality of the digital signals. The method of claim 74 further includes storing *for each of the two digital signals* a *respective* compensation value

indicative of the respective selected phase adjusted clock signal, and according to the *respective* compensation value stored for each of the two digital signals, applying *the selected phase adjusted clock signal* as the respective timing clock signal. As previously discussed with respect to claim 67, neither the Zerbe or Dow patent disclose or contemplate this level of timing adjustability. The adjusted TCLK and RCLK signals according to the Zerbe and Dow patent are used for timing the transmission and reception of all the data signals and not data signals individually. Consequently, it is still possible for one of the data signals to be skewed to such an extent that its data eye does not overlap with the data eyes of the rest of the data signals.

For the foregoing reasons, claims 67 and 74 are patentably distinct from both the Zerbe patent and the Dow patent. Claims 68-73, which depend from claim 67, and claims 75-80, which depend from claim 74, are similarly patentably distinct based on their dependency from a respective allowable base claim. Therefore, the rejection of claims 67-80 under 35 U.S.C. 102(e) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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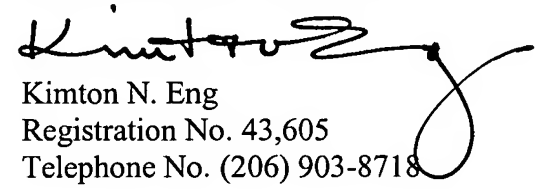

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